Nanostructure Arrays for Multijunction Solar Cells

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ABSTRACT

We are currently developing the technology for high efficiency multijunction photovoltaic cells based on semiconductor nanostructure arrays. This approach is based on electrochemical synthesis of doped II-VI semiconductor materials using a preformed template. These devices are expected to provide increased energy conversion efficiency as well as increased carrier collection efficiency. In addition, this approach provides the ability to tune the absorption spectrum to match selected windows of the solar spectrum. In this paper we will present our recent results in II-VI semiconductor quantum wire fabrication and characterization.

1. Introduction

While photovoltaic cells based on thin film technologies are among the most promising for commercial applications, many technical challenges still remain such as reduced cell efficiency, poorer material quality, spatial non-uniformity, material stability and manufacturing costs [1-4]. In order to address these limitations, we are developing a new *inexpensive* photovoltaic cell technology based on the electrochemical fabrication of semiconductor *nanostructures*. Nanostructure based PV cells have the potential to provide very high energy conversion efficiencies resulting from the following effects: (a) nanostructure *crystallite sizes* are comparable to the *carrier scattering lengths*, which significantly reduces the carrier scattering rate, thus *increasing the carrier collection efficiency*; and (b) the *strong absorption coefficient* of nanostructures due to the increased density of states. In addition, by varying the size of the nanostructures, the band gap can be tuned to absorb in a particular photon energy range [5]. The major impediment to the development of a nanostructure based PV technology has been the inability to fabricate large arrays of nanostructures with the required periodicity and size control at low cost. We have developed a unique low cost technology for the fabrication of periodic arrays of semiconductor nanostructures with very good size control (± 10%) and periodicity. This technique uses electrochemical synthesis on a preformed template of anodized aluminum to form the nanostuctures (Figure 1a). This technology is also ideally suited for the formation of multijunction structures which will further increase the photo-conversion efficiency [6]. The photovoltaic cells fabricated using this technique can be formed by stacking layers of nanostructure arrays as shown in Figure 1b, where the multi-junction feature is achieved by using band gap tuning through nanostucture size control.

2. Results and Analysis

The Nanostructures Research Group, in collaboration with the University of Notre Dame has developed a process for the fabrication of highly ordered pores on a silicon substrate and for direct-current, underpotential deposition of CdS quantum wires into these pores. A top FESEM view of the pore order is shown in Figure 2. This template structure was created through the single-step anodization of a 500 nm thick 99.999% Al film deposited by e-beam evaporation.

One important concern for devices that rely on charge transport is the state of the nanostructure/silicon interface. During template formation, a barrier layer with thickness approximately equal to the pore diameter remains after the anodization process is completed. A second concern is that anodic oxidation of the silicon surface will occur leading to the formation of an insulating silicon dioxide layer at this interface. To alleviate these concerns, an Al/Pt/Si structure has been developed by WVU and Notre Dame [7,8] that provides *in situ* barrier layer removal and prevents anodic oxidation of the silicon surface. Cross-sectional FESEM images of this interface along with the initial stages of CdS formation are shown in Figures 3 and 4. The *in situ* barrier layer removal process is significant since this can enable the use of underpotential, direct-current electrochemical deposition. The use of these techniques has been demonstrated to substantially improve semiconductor material quality.

Photoluminescence (PL) characterization on the initial CdS samples grown using this technique are shown in Figure 5. The PL shows a strong peak near mid-gap, most likely from vacancy sites, as well as a band-edge luminescence that is blue shifted. The results of Raman measurements on CdS quantum wires with diameters of 40 nm (sample 1) and15 nm (sample 2) are shown in Figures 6 and 7. The 15 nm diameter wire shows significant enhancement in Raman scattering at the wavenumber of the first LO phonon in bulk CdS (300 cm^{-1}). For the 40 nm sample, somewhat weak scattering is observed at approximately 313 cm^{-1}. The broad peak in the range between 1000-4000 cm^{-1} has been attributed to inter-subband transitions. This feature is not observed in the 40 nm sample and seems to indicate the onset of quantum confinement for the 15 nm diameter sample. The series of sharp lines around 1300 cm^{-1} is believed to be due to luminescence from trace amounts of rare earth impurities.

3. Discussion

An important advance in this research has been the development of a "barrier engineering" process to eliminate the alumina barrier layer *in situ*. Previously, this was accomplished with a phosphoric acid etch that provided a very narrow process window between incomplete barrier etching and template lift-off. The ability to remove the barrier layer in a controlled fashion enables the use of underpotential DC

deposition techniques that provide the promise to substantially improve deposited semiconductor material quality. The use of these techniques to fabricate alternate semiconductor materials (CdSe, CdTe) and material heterojunctions will be the focus of the next research phase.

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FIGURES

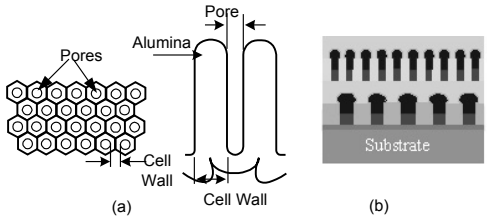

Fig. 1 (a) Top and cross-sectional views of template, and (b) schematic cross-section of nanostrcuture multijunction PV cell.

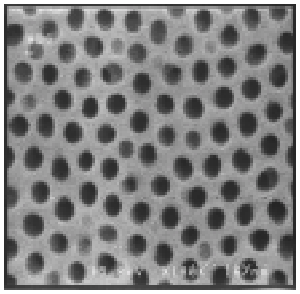

Fig. 2 Top view of alumina pores on a silicon substrate.

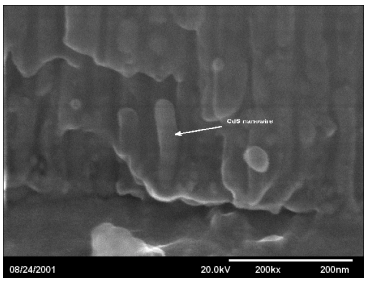

Fig 3. Cross sectional view of Al/Pt/Si structure showing initial stages of CdS synthesis.

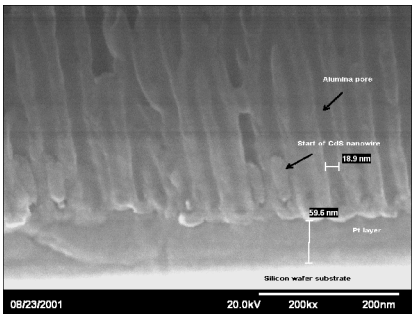

Fig. 4 Cross-sectional view of Al/Pt/Si showing the alumina/Pt interface.

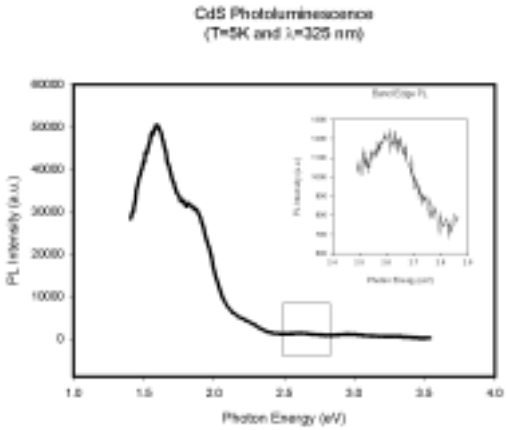

Fig. 5 PL measurements of CdS quantum wires. The inset shows the band-edge luminescence with a slight blue-shift.

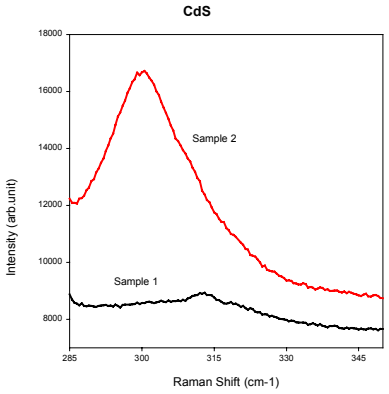

Fig 6 Raman measurements of CdS quantum wires near the first LO phonon in bulk CdS.

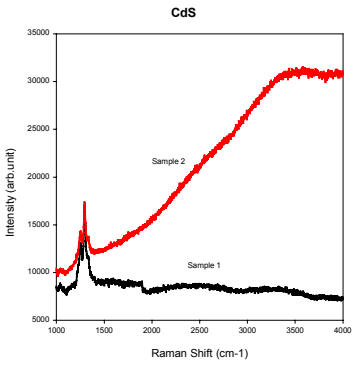

Fig 7 Raman measurements in the range of 1000-4000 cm^{-1}